High-Isolation Bonding Pad with Depletion-Insulation Structure for RF/Microwave Integrated Circuits on Bulk Silicon CMOS

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Abstract — **Bonding pads for RF/microwave integrated circuits on bulk silicon CMOS is designed with a simple depletion-insulation (DI) structure. Experimental results show high isolation and low substrate loss. An inter-pad isolation of more than 40dB at 10GHz is obtained for a 90-μm separation distance. The isolation is about two orders of magnitude higher than that of the conventional structure. The return loss is also less than 1.5dB at 10GHz. The high *Q* factor of the DI pad is achieved a few times greater that of the conventional type. The low pad capacitance of about 0.013fF/μm² is attained. This will increase the resonant frequency of the bond-wire-pad connection. The application of the useful DI structure is extendable to interconnect and planar spiral inductor to reduce the substrate loss and increase the *Q* factor.**

I. INTRODUCTION

Driven by the strong demand for low-cost wireless personal communication systems, CMOS radio-frequency integrated circuits (RFIC) or silicon monolithic microwave integrated circuits (MMIC) have been of increasing importance due to its advantages of low fabrication cost and high level integration with the digital VLSI circuits. However, in the silicon-based RFIC or MMIC, the semiconducting silicon substrate has been a major problem towards the monolithic integration of wireless chip [1]. The silicon substrate makes high frequency isolation difficult due to cross-talk through the semiconducting substrate on which both active and passive devices are fabricated. In addition, the substrate loss in silicon RFIC jeopardize the overall circuit performance as frequency becomes higher and higher. The problem is more severe in passive components using metal interconnect such as bonding pads, planar inductor and overlay capacitor. Among these passive elements, the issue is especially subtle for bonding pads because almost all integrated circuits require the essential bonding pads to interface the connections between the circuits on chip and the external circuits with various packaging technologies such as wire bonding. With its large metal plate area, typically 100μm×100μm, the substrates effects through the bonding pads can be so damaging that even the performance gain in the design optimization at the circuit level cannot compensate the loss due to the bonding pads. Unfortunately, this issue is overlooked quite often.

In order to tackle the lossy substrate problem in the bonding pads, several techniques has been used. The most common one is the use of a ground-shielding (GS) plate underneath the pad. This technique does gives some beneficial effects, namely excellent isolation [2-3] and lowered noise figure [3-4]. However, this structure requires a process with higher metallization level as it has to use the topmost metal layer for bonding pads so that the pad capacitance can be minimized. Otherwise, the fewer metallization level of the process has, the higher is the pad capacitance which implies a lower maximum operation frequency of the bonding pads (Fig. 1). Typically, a GS bonding pad can have a pad capacitance as high as 0.35pF for a typical pad size of 100μm×100μm. Assuming a 2mm long bond wire connected to the GS bonding pad, the inductance (≈ 2nH) [5] of the bond wire will resonate with the pad capacitance at about 6GHz as

$$f_{resonant} = 1/2\pi\sqrt{LC}$$

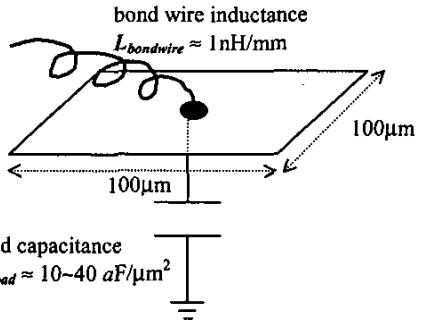

Fig. 1 The schematic picture showing the high frequency connection of a bond wire to a bonding pad.

Definitely, the lower resonant frequency can kill the high frequency connection of the bonding pad hence the overall performance of the circuit chip. Furthermore, this

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GS technique is not extendable to other metal-interconnect passive components such as planar spiral inductor [6].

In this paper, a bonding pad with simple depletion-insulation (DI) structure is designed to achieve high isolation, low substrate loss and low pad capacitance yet requires no advanced CMOS processes with high metallization level. The technique is also useful for other passive components with metal interconnect to suppress the insertion loss and raise the Q-factor.

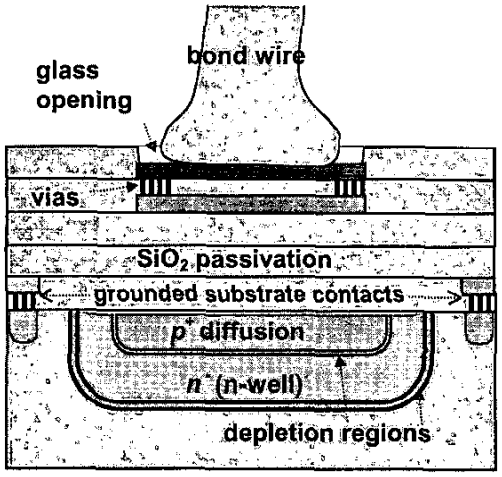

Fig. 2 The cross-section of the bonding pads with depletion-insulation structure

II. Depletion-Insulation (DI) Bonding Pad

The proposed bonding pad with DI structure is shown in Fig. 2. The two topmost metal layers are used to construct the bonding pads with many small contact vias on the perimeter connecting the two metal layers. The contact vias are to prevent lift-off during wire bonding. Right underneath the bonding pad, there is a large p-diffusion layer embedded in an even larger n-well in the silicon substrate. This structure of p-diffusion–n-well–p-substrate will form two p-n junctions. Due to the carrier depletion in the p-n junction, a sandwiched insulating depletion layer is formed. Hence, two junction capacitors are introduced in series the pad capacitance to the substrate. The technique has been used to attain a low-capacitance I/O connection [7]. However, this low capacitance is not sufficient to suppress the substrate coupling in RFIC. A large number of grounded substrate contacts surrounding the pad have to be added to increase the isolation (Fig. 2).

With an approximation of abrupt junction in the DI structure, the junction capacitance per unit area and the corresponding depletion width are respectively given by

$$C_j = \sqrt{\frac{q\varepsilon_{Si}N_A N_D}{2\phi_{bi}(N_A+N_D)}}\sqrt{\frac{\phi_{bi}}{(\phi_{bi}-V_R)}}$$

$$W_{di} = \sqrt{\frac{2\varepsilon_{Si}(N_A+N_D)(V_R+\phi_{bi})}{qN_A N_D}}$$

Considering the respective doping concentrations of p-substrate, n-well and p-diffusion with typical values of $N_{A\_sub} = 10^{15}\text{cm}^{-3}$, $N_{D\_n\text{-well}} = 10^{16}\text{cm}^{-3}$, and $N_{A\_p\text{-diff}} = 10^{17}\text{cm}^{-3}$, the junction capacitances are 0.1 fF/μm^2 and 0.3 fF/μm^2 while the depletion widths are 9000 Å and 3000 Å. The two series capacitances lower the pad capacitance. More importantly, the two thick layer of insulating depletion region of the p-n junctions make it equivalent to that the lossy silicon substrate is partially "removed" but without using any high-cost micromachining or SIMOX technologies yet achieving the similar insulating effect. This simple DI technique can be realized in any bulk CMOS technology with almost zero cost.

In the design of this DI bonding pad in a standard CMOS process, an active mask layout has to be drawn together with the p-select mask layout so that the p implantation can be injected into the n-well. Otherwise, if without the active mask, field oxide will form on the surface of the n-well and block the p^+ implant resulting in null formation of p-diffusion.

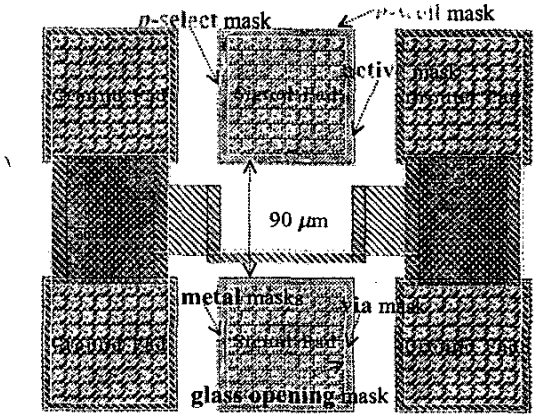

Fig. 3 The ground-signal-ground test structure of the DI bonding pads.

III. Experimental Results & Discussion

The DI bonding pads have been fabricated using a commercially available 0.35-μm CMOS process. The pads are configured in a standard ground-signal-ground layout (Fig. 3). The capacitance is measured with LCR

impedance analyzer while the microwave S-parameter measurements of the pads are performed with HP8510C vector network analyzer and Cascade microwave air-coplanar probes with SOLT calibration. The results are compared with those of conventional bonding pads.

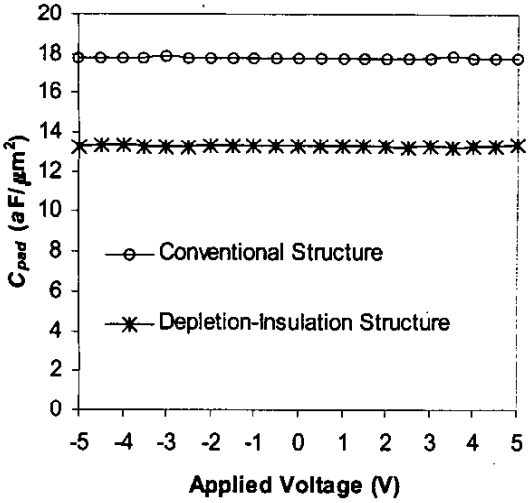

Fig. 4 The measured pad capacitance (per unit pad area) of the DI bond pads compared with the conventional type.

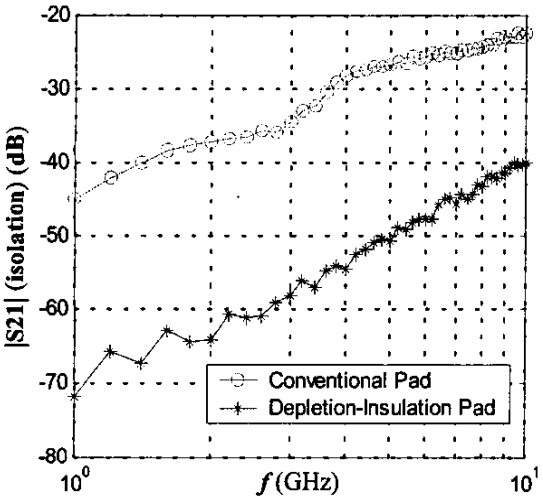

Fig. 5 The higher inter-pad isolation of the DI bonding pads compared with the conventional type.

From the measured pad capacitance, the DI bonding pads gives almost 30% reduction in the pad capacitance per unit pad area compared with the conventional pad structure (Fig. 4). This is entirely due to the additional junction capacitances in the signal path from the bonding pad to the substrate as explained in the previous section. The reduction in the capacitance can be even larger if the process allows p^+ implant before field oxidation so that another field oxide capacitance can be added in series.

With the two port S-parameter measurement of the ground-signal-ground test structure, the isolation of the bonding pads is obtained as shown in Fig. 5. The inter-pad isolation of the DI bonding pad is about 40dB at 10GHz, about two orders of magnitude higher than that of the conventional type. The high isolation can be attributed to the insulating depletion layer and the surrounding grounded substrate contacts in the substrate.

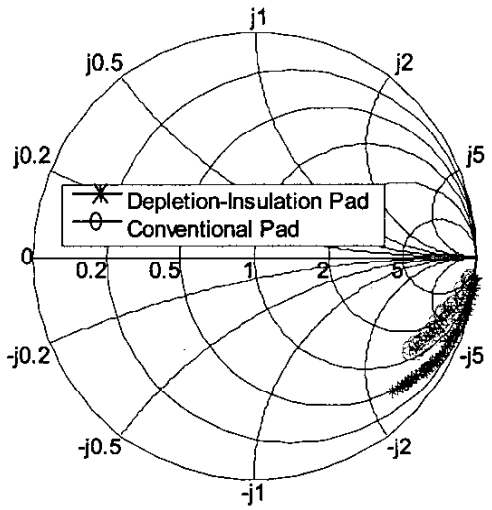

Fig. 6 The Smith chart representation of the 1-port measurement result of the DI bonding pads compared with the conventional type.

Apart from the isolation improvement, the substrate loss of the DI bonding pads is also minimized. This can be reflected from the one-port measurement of the bonding pads. The Smith chart representation of the bonding pad one-port measurement is shown in Fig. 6. The normalized resistance of the bonding pad is smaller for the DI type. This implies a possible lower energy loss of the DI bonding pads. This can be verified by looking at the return loss and the Q-factor of the bonding pad. In Fig. 7, the return loss of the DI pad is smaller while the Q-factor of the pad is higher in Fig. 8. Both two pieces of experimental results indicate an improved substrate loss to the substrate. Again, as explained previously, this is mainly due to the thick depletion-insulation layers of the

p-n junctions formed underneath the bonding pad. It is effectively as if part of the lossy silicon substrate is removed by making it insulating. This results in smaller substrate loss to the substrate. The extracted series substrate resistance based on first order model shows smaller values of the DI bonding pad (Fig. 9) provides the self-explanatory answer.

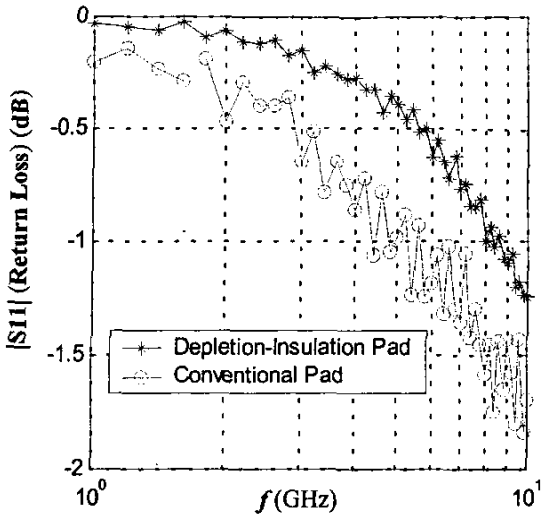

Fig. 7 The measured smaller return loss of the DI bonding pads compared with the conventional type.

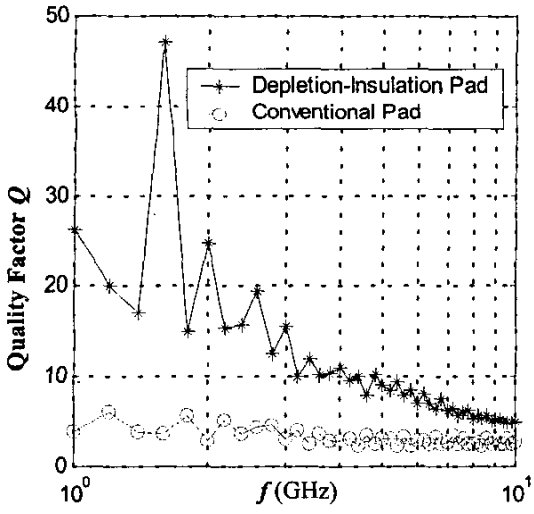

Fig. 8 The measured better Q-factor of the DI bonding pads compared with the conventional type.

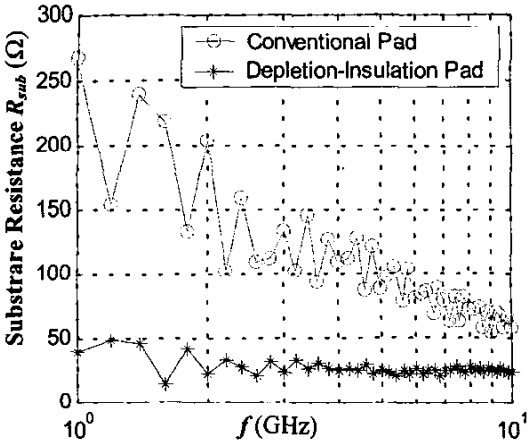

Fig. 9 The extracted substrate resistance of the DI bonding pads compared with the conventional type.

IV. Conclusion

The high-isolation bonding pad on bulk silicon CMOS is achieved easily with a depletion-insulation structure. By making part of the silicon substrate insulating, the inter-pad isolation and the *Q*-factor of bonding pads are significantly raised. The structure can be used in other silicon MMIC components to either isolate it from substrate coupling or reduces the substrate loss.

Acknowledgement

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References

[1] R. C. Frye, "Integration and electrical isolation in CMOS mixed-signal wireless chips", *Proc. of IEEE*, vol. 89, April 2001, pp. 444-455.

[2] T. E. Kolding, "Shielded-based microwave on-wafer device measurements", *IEEE Tran. on Microwave Theory and Tech*, vol. 49, no. 6, June 2001, pp. 1039-1044.

[3] J. T. Colvin, S. S. Bhatia, and K. K. O, "A bond-pad structure for reducing effects of substrate resistance on LNA performance in a silicon bipolar technology", *Proc. of 1998 Bipolar Cir. Tech. Meeting*, 1998, pp. 109-122.

[4] N. Camilleri, J. Kirchgessner, J. Costa, D. Ngo, and D. Lovelace, "Bonding pad models for silicon VLSI technologies and their effects on the noise figure of RF NPNs", 1994 *Int. Microwave Symp. Dig*, pp. 1179-1182.

[5] J. M. Rabaey, *Digital Integrated Circuits: a Design Perspective*, Upper Saddle River, NJ: Prentice Hall, 1996.

[6] C. P. Yue, and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-Based RF IC's", *IEEE J. of Solid-State Circuits*, vol. 33, May 1998, pp. 743-752.

[7] M.-D. Ker, H.-C. Jiang, and C.-Y. Chang, "Design of low-capacitance bond pad for high frequency I/O applications in CMOS integrated circuits", *Proc. of 13th Annual IEEE Int. ASIC/SOC Conference*, 2000, pp. 293-296.